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| 10/075,181 | 02/13/2002 | Shane Clifford | 303.759US1 | 7264 |

| | | | EXAMINER |
|---|---|---|---|
| 21186 | 7590 | 12/05/2006 | YIGDALL, MICHAEL J |

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| 2192 | |

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- . If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>07 September 2006</u>.

2a)☒ This action is **FINAL.**      2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5-7,9-12,14-20,22-26,28-32,34-38 and 40-51* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9-12,14-20,22-26,28-32,34-38 and 40-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
      Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
      Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 08-06)          Office Action Summary          Part of Paper No./Mail Date 20061127

## DETAILED ACTION

1.      This Office action is responsive to Applicant's submission filed on September 7, 2006.

Claims 1-3, 5-7, 9-12, 14-20, 22-26, 28-32, 34-38 and 40-51 are pending.

### *Response to Amendment*

2.      The rejection of claim 44 under 35 U.S.C. 101, as set forth in the Office action mailed on

June 7, 2006, is withdrawn in view of Applicant's amendment.

### *Response to Arguments*

3.      Applicant's arguments have been fully considered but they are not persuasive.

Applicant contends that the combination of Coad and Takano is based on an improper

*prima facie* showing of obviousness because there is no teaching or suggestion within Coad or

Takano to make the combination (remarks, pages 11-12).

However, the examiner does not agree with Applicant's conclusions.  It is noted that

obviousness can only be established by combining or modifying the teachings of the prior art to

produce the claimed invention where there is some teaching, suggestion, or motivation to do so

found either in the references themselves or in the knowledge generally available to one of

ordinary skill in the art.  See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In

re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Here, Coad is directed to a software development system that conforms to the Unified

Modeling Language (see, for example, column 15, lines 50-54).  Coad discloses that UML is

used to model real-time systems (see, for example, column 1, lines 47-52).  Thus, Coad teaches a

software development system for modeling a real-time system.  While Coad is silent as to a real-

time system for controlling semiconductor fabrication equipment (i.e., the intended use recited in

the claims), Takano expressly discloses a control system for controlling semiconductor

fabrication equipment (see, for example, column 8, lines 2-23). Similarly to Coad, Takano is

directed to the development of software for such control systems (see, for example, the abstract).

Thus, Takano's teachings are a suggestion to apply Coad's software development system to a

real-time system whose intended use is for controlling semiconductor fabrication equipment.

Accordingly, as set forth in the Office action, modeling a system for controlling semiconductor

fabrication equipment would have been obvious to a person having ordinary skill in the art in

view of Coad and Takano.

### *Claim Rejections - 35 USC § 103*

4.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

5.      Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S.

Patent No. 6,851,107 to Coad et al. (art of record, "Coad") in view of U.S. Patent No. 6,591,152

to Takano (art of record, "Takano") in view of U.S. Patent No. 6,179,490 to Pruitt (art of record,

"Pruitt").

With respect to claim 1 (previously presented), Coad discloses a computerized method

for utilizing a feature diagram in the creation of a potential statechart (see, for example, column

4, lines 38-45, which shows developing software by creating corresponding graphical

representations of the source code, and column 17, lines 16-22 and 37-42, which shows that the

graphical representations include statecharts and component diagrams, i.e. feature diagrams),

comprising:

(a) adding a state to the potential statechart for each state-type feature added to the

feature diagram (see, for example, column 4, line 61 to column 5, line 3, which shows updating

the graphical representations when changes are made to the code, and FIG. 16, which shows

states that are added to the statechart).

Although Coad discloses that the feature diagram models a real-time control system (see,

for example, column 1, lines 47-52), Coad does not expressly disclose that the feature diagram

models a system for controlling semiconductor equipment used to process a Lot of

semiconductor wafers.

However, Takano discloses modeling a system (see, for example, the abstract), including

a system for controlling semiconductor equipment used to process a Lot of semiconductor wafers

(see, for example, column 8, lines 2-23).

It would have been obvious to one of ordinary skill in the art at the time the invention

was made to apply the method of Coad to a system for controlling semiconductor equipment

used to process a Lot of semiconductor wafers, such as suggested by Takano.

Although Coad discloses that the statecharts illustrate states and transitions (see, for

example, column 17, lines 16-22), including decision states (see, for example, FIG. 17 and

column 17, lines 25-32), Coad in view of Takano does not expressly disclose:

(b) for each added state-type feature that is an optional feature, adding a decision state to the potential statechart that has a guarded transition to the added state and adding an else transition;

(c) for each alternate relationship to be added to the feature diagram, adding a decision state to the potential statechart and adding a guarded transition from the added decision state to each of the states in the alternate relationship, wherein an else transition is added to the added decision state if the features in the alternate relationship are optional; and

(d) for each or-relationship to be added to the feature diagram, adding a decision state to the potential statechart for each state in the or-relationship, wherein each added decision state has a guarded transition to one of the states in the or-relationship, and each decision state has an else transition.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add the appropriate states to the statechart of Coad in a manner so as to reflect the desired relationships.

Moreover, Pruitt discloses an analogous method for creating a flowchart to represent and create a program (see, for example, column 1, lines 8-15). Programs created in this manner are "structured" so as to improve the quality of the program (see, for example, column 2, lines 1-5).

Pruitt further discloses elements of the flowcharts, such as "if-then" and "if-then-else" blocks for "optional" and "alternate" relationships (see, for example, FIGS. 2D and 2E), as in parts (b) and (c) above, and "case" blocks for "or" relationships (see, for example, FIG. 2F), as in part (d) above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the method of Coad and Takano with such features as taught by Pruitt, so as to create programs that are structured and therefore of improved quality.

With respect to claim 2 (previously presented), the rejection of claim 1 is incorporated, and Coad also discloses the limitation wherein the potential statechart conforms to the Unified Modeling Language (see, for example, column 15, lines 50-54).

With respect to claim 3 (previously presented), the rejection of claim 1 is incorporated, and Coad also discloses the limitation wherein the feature diagram models a real-time control systems (see, for example, column 1, lines 47-52).

With respect to claim 5 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 1 (see the rejection of claim 1 above). Coad also discloses:

(e) adding transitions to the potential statechart, wherein the transitions are transitions that are triggered by a signal or stimulus (see, for example, column 17, lines 16-22, which shows transitions caused by stimuli).

With respect to claim 6 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 2 (see the rejection of claim 2 above).

With respect to claim 7 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 3 (see the rejection of claim 3 above).

6.      Claims 9-12, 14-20, 22-26, 28-32, 34-38 and 40-51 are rejected under 35 U.S.C. 103(a)

as being unpatentable over Coad in view of Takano in view of U.S. Patent No. 5,825,651 to

Gupta et al. (art of record, "Gupta").

With respect to claim 9 (currently amended), Coad discloses a computerized method (see,

for example, the abstract), comprising:

(a) creating a feature diagram and a corresponding potential statechart (see, for example,

column 4, lines 38-45, which shows developing software by creating corresponding graphical

representations of the source code, and column 17, lines 16-22 and 37-42, which shows that the

graphical representations include statecharts and component diagrams, i.e. feature diagrams).

Although Coad discloses that the feature diagram models a system for controlling a real-

time system (see, for example, column 1, lines 47-52), Coad does not expressly disclose the

limitation wherein the feature diagram models a system for controlling semiconductor

fabrication equipment.

However, Takano discloses modeling a system (see, for example, the abstract), including

a system for controlling semiconductor fabrication equipment (see, for example, column 8, lines

2-23).

It would have been obvious to one of ordinary skill in the art at the time the invention

was made to apply the method of Coad to a system for controlling semiconductor fabrication

equipment, such as suggested by Takano.

Coad also discloses:

(b) modifying the feature diagram (see, for example, column 4, line 61 to column 5, line

3, which shows changing a graphical representation of the code).

Coad in view of Takano does not expressly disclose selecting one or more features from a universe of predefined features.

However, Gupta discloses configuring a system (see, for example, column 4, lines 31-32), including selecting one or more features from a universe of predefined features (see, for example, column 8, lines 12-27), so as to ensure compatibility among features and that the system is valid (see, for example, column 5, line 63 to column 6, line 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the method of Coad and Takano with feature selections such as taught by Gupta, so as to ensure that the modifications to the feature diagram are valid.

Coad also discloses:

(c) making modifications to the potential statechart that correspond to the modifications of the feature diagram to produce a deterministic statechart (see, for example, column 4, line 61 to column 5, line 3, which shows updating the graphical representations when changes are made to the code, and column 17, lines 25-32, which shows an activity diagram, i.e. a deterministic statechart).

With respect to claim 10 (previously presented), the rejection of claim 9 is incorporated, and Coad also discloses the limitation wherein the potential statechart conforms to the Unified Modeling Language (see, for example, column 15, lines 50-54).

With respect to claim 11 (previously presented), the rejection of claim 9 is incorporated, and Coad also discloses the limitation wherein the deterministic statechart conforms to the Unified Modeling Language (see, for example, column 15, lines 50-54).

With respect to claim 12 (previously presented), the rejection of claim 9 is incorporated, and Coad also discloses the limitation wherein the feature diagram models a real-time control system (see, for example, column 1, lines 47-52).

With respect to claim 14 (previously presented), the rejection of claim 9 is incorporated, and Coad also discloses the limitation wherein computer-executable code is generated as a function of the deterministic statechart (see, for example, column 5, lines 10-13).

With respect to claim 15 (previously presented), the rejection of claim 9 is incorporated, and Coad also discloses the limitation wherein computer-executable code for a real-time control system is generated as a function of the deterministic statechart (see, for example, column 5, lines 10-13, and column 1, lines 47-52).

With respect to claim 16 (previously presented), the rejection of claim 9 is incorporated, and Coad in view of Takano also discloses the limitation wherein computer-executable code for a system for controlling semiconductor equipment is generated as a function of the deterministic statechart (see, for example, column 5, lines 10-13, and column 1, lines 47-52).

With respect to claim 17 (currently amended), the limitations recited in the claim correspond to the limitations recited in claim 9 (see the rejection of claim 9 above). Coad also discloses:

(d) generating computer-executable code from the deterministic statechart (see, for example, column 5, lines 10-13).

With respect to claim 18 (original), the limitations recited in the claim correspond to the limitations recited in claim 10 (see the rejection of claim 10 above).

With respect to claim 19 (original), the limitations recited in the claim correspond to the limitations recited in claim 11 (see the rejection of claim 11 above).

With respect to claim 20 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 12 (see the rejection of claim 12 above).

With respect to claim 22 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 14 (see the rejection of claim 14 above).

With respect to claim 23 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 15 (see the rejection of claim 15 above).

With respect to claim 24 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 16 (see the rejection of claim 16 above).

With respect to claim 25 (currently amended), the limitations recited in the claim correspond to the limitations recited in claim 17 (see the rejection of claim 17 above).

With respect to claim 26 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 15 (see the rejection of claim 15 above).

With respect to claim 28 (original), the limitations recited in the claim correspond to the limitations recited in claim 11 (see the rejection of claim 11 above).

With respect to claim 29 (previously presented), the limitations recited in the claim

correspond to the limitations recited in claim 12 (see the rejection of claim 12 above).

With respect to claim 30 (previously presented), the rejection of claim 25 is incorporated,

and Takano further discloses the limitation wherein the feature diagram models a system for

controlling semiconductor equipment (see, for example, column 8, lines 2-23).

With respect to claim 31 (currently amended), Coad discloses a system useful for

generating computer-executable code (see, for example, column 5, lines 10-13), comprising:

(a) a repository having stored feature diagrams and corresponding potential statecharts

(see, for example, column 4, lines 38-45, which shows developing software by creating

corresponding graphical representations of the source code, and column 17, lines 16-22 and 37-

42, which shows that the graphical representations include statecharts and component diagrams,

i.e. feature diagrams; also see, for example, column 15, lines 61-64, which shows using existing

code, i.e. stored code).

Although Coad discloses that the feature diagram models a system for controlling a real-

time system (see, for example, column 1, lines 47-52), Coad does not expressly disclose the

limitation wherein the feature diagrams model a system for controlling semiconductor

fabrication equipment.

However, Takano discloses modeling a system (see, for example, the abstract), including

a system for controlling semiconductor fabrication equipment (see, for example, column 8, lines

2-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method of Coad to a system for controlling semiconductor fabrication equipment, such as suggested by Takano.

Coad also discloses:

(b) an editor capable of making modifications to the stored feature diagrams and capable of making modifications to the potential statecharts that correspond to modifications made to the stored feature diagrams (see, for example, column 4, line 61 to column 5, line 3, which shows changing a graphical representation of the code and updating the graphical representations when changes are made to the code).

Coad in view of Takano does not expressly disclose that the editor is adapted to allow selection of one or more features to be included in a statechart from a universe of predefined features.

However, Gupta discloses configuring a system (see, for example, column 4, lines 31-32), including an editor that allows selection one or more features from a universe of predefined features (see, for example, column 8, lines 12-27), so as to ensure compatibility among features and that the system is valid (see, for example, column 5, line 63 to column 6, line 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the system of Coad and Takano with feature selections such as taught by Gupta, so as to ensure that the modifications to the statechart are valid.

With respect to claim 32 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 12 (see the rejection of claim 12 above).

With respect to claim 34 (original), the limitations recited in the claim correspond to the limitations recited in claim 12 (see the rejection of claim 12 above).

With respect to claim 35 (original), the rejection of claim 31 is incorporated, and Takano further discloses the limitation wherein the stored feature diagrams and corresponding potential statecharts are useful for modeling a system for controlling semiconductor equipment (see, for example, column 8, lines 2-23).

With respect to claim 36 (original), the limitations recited in the claim correspond to the limitations recited in claim 10 (see the rejection of claim 10 above).

With respect to claim 37 (currently amended), the limitations recited in the claim correspond to the limitations recited in claim 31 (see the rejection of claim 31 above). Coad also discloses:

(d) a code generator for generating computer-executable code from deterministic statecharts (see, for example, column 5, lines 10-13).

With respect to claim 38 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 15 (see the rejection of claim 15 above).

With respect to claim 40 (original), the limitations recited in the claim correspond to the limitations recited in claims 10 and 11 (see the rejection of claims 10 and 11 above).

With respect to claim 41 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 12 (see the rejection of claim 12 above).

With respect to claim 42 (previously presented), the rejection of claim 37 is incorporated, and Takano further discloses the limitation wherein the stored feature diagrams model one or more systems for controlling semiconductor equipment (see, for example, column 8, lines 2-23).

With respect to claim 43 (currently amended), the limitations recited in the claim correspond to the limitations recited in claim 9 (see the rejection of claim 9 above).

With respect to claim 44 (currently amended), the limitations recited in the claim correspond to the limitations recited in claim 9 (see the rejection of claim 9 above).

With respect to claim 45 (currently amended), the limitations recited in the claim correspond to the limitations recited in claim 9 (see the rejection of claim 9 above).

With respect to claim 46 (previously presented), the rejection of claim 9 is incorporated, and Gupta further discloses the limitation wherein the universe of predefined features includes one or more required features (see, for example, column 6, lines 32-37, which shows an "includes" relation among the features).

With respect to claim 47 (previously presented), the rejection of claim 9 is incorporated, and Gupta further discloses the limitation wherein the universe of predefined features includes two or more mutually exclusive features (see, for example, column 6, lines 37-43, which shows a "can't work with" or "excluded" relation among the features).

With respect to claim 48 (previously presented), the rejection of claim 9 is incorporated, and Gupta further discloses the limitation wherein the universe of predefined features includes a

group of two or more features, at least one of which must be included in the feature diagram (see, for example, column 6, lines 50-59, which shows a "requires choice" relation among the features).

With respect to claim 49 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 46 (see the rejection of claim 46 above).

With respect to claim 50 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 47 (see the rejection of claim 47 above).

With respect to claim 51 (previously presented), the limitations recited in the claim correspond to the limitations recited in claim 48 (see the rejection of claim 48 above).

*Conclusion*

7.      Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

8.      Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707.

The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you

would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MY                          Michael J. Yigdall
                            Examiner
                            Art Unit 2192

mjy

TUAN DAM
SUPERVISORY PATENT EXAMINER